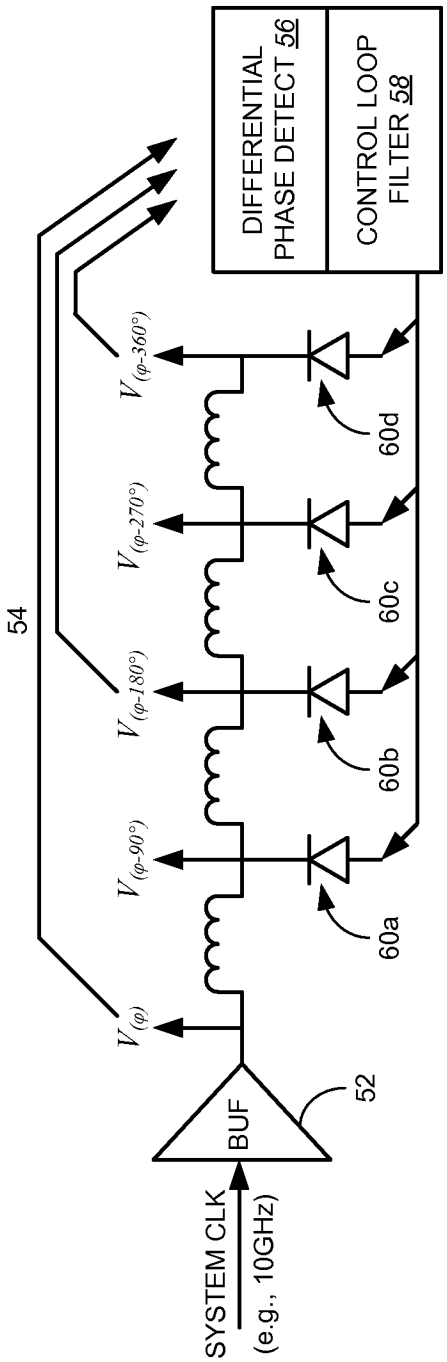

SYSTEM CLK
(e.g., 10GHz)
BUF
52
$V_{(\varphi)}$
$V_{(\varphi-90°)}$
$V_{(\varphi-180°)}$
$V_{(\varphi-270°)}$
$V_{(\varphi-360°)}$
60a
60b
60c
60d
54
DIFFERENTIAL PHASE DETECT 56
CONTROL LOOP FILTER 58

50

FIG. 3

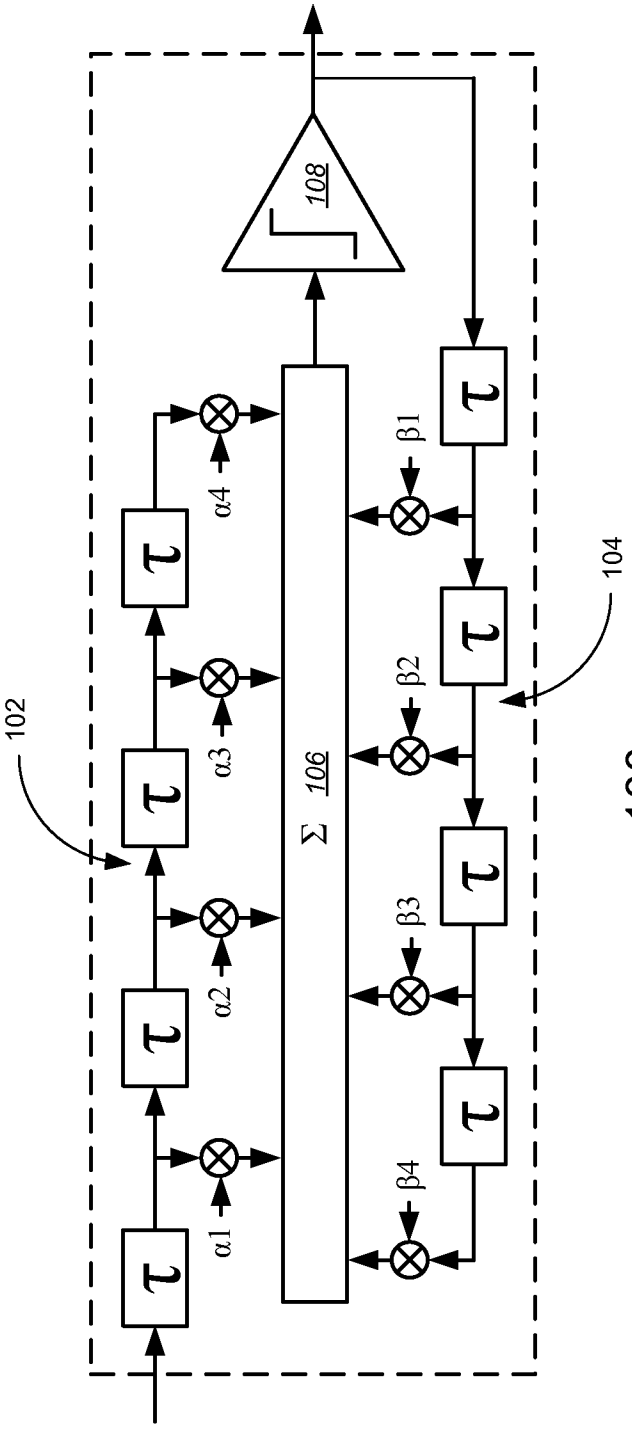
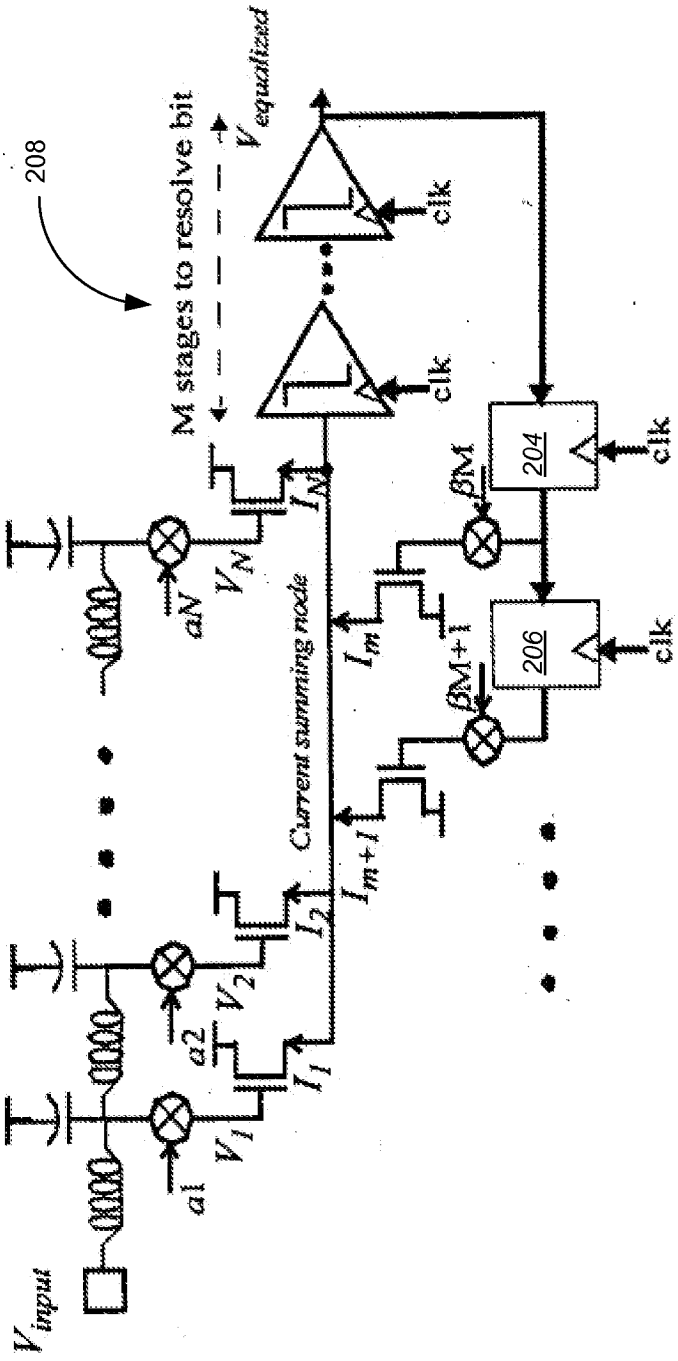


FIG. 5


208
M stages to resolve bit
$V_{equalized}$
clk
V_{input}
a1
a2
aN
V_1
V_2
V_N
I_1
I_2
I_N
Current summing node
I_m
I_{m+1}
βM
βM+1
204
206

300

FIG. 7